REMARKS

Applicants gratefully acknowledge Examiner Vicary for taking time from his busy schedule on June 15, 2007, to conduct a telephone interview with co-inventor Gustavson, IBM patent attorney Kaufman, and Applicants' representative Cooperrider. Applicants believe that the interview was productive and will greatly expedite prosecution. Applicants were also very impressed by the quality of the evaluation for this application by Examiner Vicary.

During the interview, Examiner Vicary indicated that he thought the 35 U.S.C. § 101 rejection would not be maintained, based on recent clarifications within the USPTO. The Examiner also indicated that changing the independent claim preamble to describe "method of increasing efficiency/speed" would not be necessary and might raise an indefiniteness issue.

Dr. Gustavson provided a summary of the present invention, starting out by explaining that preloading and prefetching were usually considered in the art as two different processes. That is, preloading involves data exchange between cache L1 and the FPU register file, which IBM calls "L0", whereas prefetching involves getting data into the L1 cache.

Claims 1-20 are all the claims presently pending in the application, with claim 20 being added.

It is noted that Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-19 stand rejected under non-statutory double patenting over claims 1, 3-6, 8-12, and 14-19 of co-pending application S/N 10/671,937. Claims 1-5 and 11-19 stand rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Claims 1-5 and 12-19 stand rejected under 35 U.S.C. § 101 as directed toward non-statutory subject matter. Claims 1-19 stand rejected under 35 U.S.C. § 102(b) as anticipated by "Superscalar GEMM-based Level 3 BLAS – The On-going Evolution of a Portable and High-Performance Library" by Gustavson et al.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a method of executing a linear algebra subroutine. For an execution code controlling an operation of a floating point unit (FPU) performing a linear algebra subroutine execution, instructions are inserted to timely move data into a cache providing data for the FPU, thereby improving an efficiency for the linear algebra subroutine execution.

Conventional compilers do not have the capability to automatically pre-fetch (timely move) data into the FPU for Level 3 Dense Linear Algebra Subroutines.

The claimed invention, on the other hand, teaches how to modify a conventional compiler to incorporate linear algebra theory and techniques to be able to automatically insert move type instructions into time slots existing in such Level 3 subroutines.

II. THE DOUBLE PATENT REJECTION

In accordance with the discussion during the telephone interview, Applicants believe the distinction between preloading and pre-fetching, in combination with the claim revisions in the present application, provide sufficient basis to distinguish the claims of the present invention from the claims of the cited co-pending application. Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE 35 USC §112, SECOND PARAGRAPH REJECTION

Claims 1-5 and 11-19 stand rejected under 35 U.S.C. §112, second paragraph. The claims have been amended, above, to overcome this rejection. Specifically, claim 1 has been revised to eliminate reference to "unrolling" and "pre-fetch", claim 2 has been revised to eliminate reference to "utilizing time slots caused …", and various claims have been revised to address antecedent basis problems and consistent terminology.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

IV. THE REJECTION UNDER 35 U.S.C. §101

Claims 1-5 and 12-19 stand rejected under 35 U.S.C. §101. During the above-mentioned telephone interview, Applicants understood that this rejection would be reconsidered in view of recent clarifications within the USPTO, particularly in view of the discussion by Applicants that the present invention provides the real-world result of

increasing efficiency of the computer and that the linear algebra processing itself was not being claimed in the abstract.

However, the Examiner indicated that he though that the preamble for claims 12-19 should be changed to "storage medium" to preclude possible interpretation that non-tangible media were included in the claims. Applicants have amended the language in these claims.

Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

V. THE PRIOR ART REJECTION

The Examiner alleges that the article by co-inventor Gustavson teaches the claimed invention. Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by this publication.

That is, as explained during the above-mentioned telephone interview, there have been considerable architectural changes in computers since co-inventor Gustavson wrote the cited publication almost ten years ago. Indeed, co-inventor Gustavson considers this earlier paper as merely giving general ground rules, and that it provides only an overview of pre-fetching in general and does not provide sufficient details to implement the present invention.

More specifically, attached co-processors were not available at the time of this paper and there was no capability of automatic pre-fetching of data into the FPU, since compilers even today do not have the capacity to automatically insert move-type instructions into linear algebra subroutines. The present invention includes this aspect of modifying conventional compilers to incorporate such linear algebra theory and techniques, such as explained in general beginning on page 12 of the disclosure.

Because of the architectural changes and the inability of compilers to automatically insert move-type instructions into linear algebra applications, co-inventor Gustavson does not consider the present invention involving L3 pre-fetching to be obvious from this earlier paper, particularly in view of the four aspects discussed during the telephone interview:

- The number of hardware pre-fetch units are limited so that one needs to have a way to minimize the amount of pre-fetching;

- The scheduling of L3 pre-fetch instructions is a bit of an art, particularly in view of the next item;

- There is a combinatorial explosion of possible choices for placing the instructions in time slots; and

- Standard compilers do a very poor job of attempting to pre-fetch instructions for linear algebra applications or they cannot do this job at all.

Therefore, Applicants submit that there are elements of the claimed invention that are not taught or suggested by this earlier publication by Gustavson. Therefore, the Examiner is respectfully requested to withdraw this rejection.

VI. FORMAL MATTERS AND CONCLUSION

Minor errors have been corrected in the disclosure, as requested by the Examiner.

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: June 19, 2007

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CERTIFICATION OF TRANSMISSION

I certify that I transmitted electronically, via EFS, this Amendment under 37 CFR §1.116 to the USPTO on June 19, 2007.

Frederick E. Cooperrider (Reg. No. 36,769)